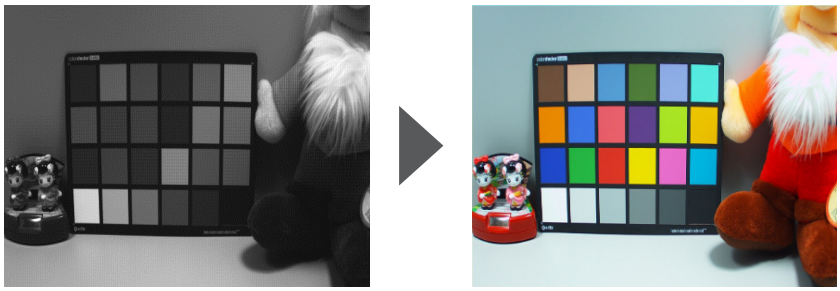
4K ISP chain using C to RTL (HLS)



BENEFITS

- 4K resolutions at 60 FPS
- Faster RTL development & verification
- Customer can focus on algorithms in CUDA/OpenCL
- Customer is offloaded from RTL development & verification

CUSTOMER CHALLENGE

Develop a Image Signal processing (ISP) chain by converting kernels from CUDA/OpenCL (currently running on GPU) to RTL using High Level Synthesizer tool from Xilinx.

SCOPE

- Conversion of image processing kernels from CUDA/OpenCL to fixed point C code.
- Conversion of fixed point C kernels to RTL using Xilinx Vivado HLS tool.
- Integration of the converted kernels to form Image Signal Processing Chain (ISP)
- Hardware validation of the converted RTL using test setup developed in Xilinx Evaluation Board (KC705)

SOLUTION

A portable standalone 4K ISP System capable of receiving input video from image sensors providing custom 4K resolutions at 60 FPS and output video with resolution of (4096 x 2160) at 60 FPS

FEATURES

- ISP processes input video in Bayer raw format and supports up to four different Bayer patterns
- ISP supports all custom input video resolutions less than (4096 x 2160).
- Other ISP features supported
  - Demosaic
  - Chrominance and Luminance noise reduction,
  - Edge Enhancement
  - Gamma Correction
  - Hue Adjustment
  - White Balance Gain Adjustment
  - Color Space conversion (RGB to YC & YC to RGB)
  - Chroma Up/Down Sampler (C444 to 422 & C422 to 444)
  - Support for Color Linear Matrix.
- ISP supports a Scaler module capable of reducing input Bayer images.

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